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November 20, 1998

Box Patent Application

BY HAND DELIVERY

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Non-Provisional Utility Patent Application
Application No.: To be Assigned; Filed: November 20, 1998
For: **Wire For Liquid Crystal Displays, Liquid Crystal Displays Having The Same, And Manufacturing Methods Thereof**
Our Ref: 06192.0052

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form;

2. Fee Transmittal Form 1082 (duplicate); and

3. U.S. Utility Patent Application entitled:
Wires For Liquid Crystal Displays, Liquid Crystal Displays Having The Same, And Manufacturing Methods Thereof

and naming as inventors:
Myung-Koo HUR
Chang-Oh JEONG

the application consisting of:

a. a specification containing:

(i) **10** pages of description prior to the claims;
(ii) 5 pages of claims (20 claims); and
(iii) a one (1) page abstract;

b. 6 sheets of drawings: (Figs. 1, 2, 3, 4A, 4B, 4C, 4D, 4E, 4F, and 5 inclusive);

4. a copy of the executed Combined Declaration and Power of Attorney for Patent Application;

5. Form PTO-1595 Recordation Cover Sheet and a copy of the executed Assignment to Samsung Electronics Co., Ltd., recordation of which is hereby respectfully requested;

6. our check no. 301583 for $956.00 to cover:

   $916.00 filing fee for patent application;
   40.00 assignment recordation fee;

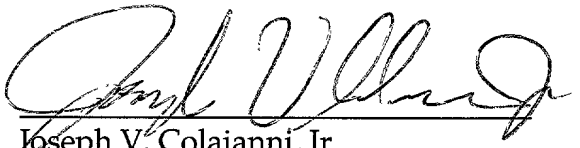
7. two (2) return postcards.

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

Applicant hereby claims foreign priority benefits under Title 35, United States Code, § 119 to Korean Application No. 97-16315 filed on November 20, 1997.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 08-3038. A duplicate copy of this letter is enclosed.

Respectfully submitted,



Joseph V. Colaianni, Jr.
Registration No. 39,948

Enclosures

PTO/SB/05 (2/98)

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Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	
Attorney Docket No.	06192.0052
First Named Inventor or Application Identifier	Myung-Koo HUR
Title	Wires For Liquid Crystal Displays, Liquid Crystal Displays Having The Same, And Manufacturing Methods Thereof
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ *Fee Transmittal Form (Form PTO-1082)
   (Submit an original and a duplicate for fee processing)
2. ☒ Specification [*Total Pages* 16]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claims
   - Abstract of the Disclosure
3. ☒ Drawing(s) *(35 USC 113)* [*Total Sheets* 6]
4. Oath or Declaration [*Total Pages*]
   - a. ☒ Newly executed (original or copy)
   - b. ☐ Copy from a prior application (37 CFR 1.63(d))
     (for continuation/divisional with Box 17 completed)
     [Note Box 5 below]
     - i. ☐ DELETION OF INVENTOR(S)
       Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   - a. ☐ Computer Readable Copy
   - b. ☐ Paper Copy (identical to computer copy)
   - c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement *(when there is an assignee)* ☒ Power of Attorney
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503) (Two)
    (should be specifically itemized)
14. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. ☐ Other:

*NOTE FOR ITEMS 1 & 14: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
    ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: /
    Prior Application Information: Examiner: Group/Art Unit:

18. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* *or* ☒ *Correspondence address below*

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FORM PTO-1082

HOWREY & SIMON
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1299 Pennsylvania Avenue, N.W.
Washington, D.C. 20004-2402
(202) 783-0800

Attorney Docket No. 06192.0052

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of
Inventor: Myung-Koo HUR and Chang-Oh JEONG
For: **Wires For Liquid Crystal Displays, Liquid Crystal Displays Having The Same, And Manufacturing Methods Thereof**

Enclosed are:
x 6 sheets of informal drawings. (Figs. 1, 2, 3, 4A, 4B, 4C, 4D, 4E, 4F, and 5, inclusive)
x An assignment of the invention to SAMSUNG ELECTRONICS CO., LTD.
___ Form PTO-1595.
___ A certified copy of _____
___ An associate power of attorney.
___ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
x Executed Power of Attorney from Assignee.
x Executed Declaration for Patent Application.

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
FOR	NO. FILED	NO. EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE				$ 380.00	OR		$ 760.00
TOTAL CLAIMS	20 -20 =	* 0	x 9 =		OR	x 18 =	
INDEP. CLAIMS	5 -3 =	* 2	x 39 =		OR	x 78 =	156.00
☐ MULTIPLE DEPENDENT CLAIM PRESENTED			+ 130 =		OR	+ 260 =	
			TOTAL		OR	TOTAL	$ 916.00

*If the difference in Col. 1 is less than zero, enter "0" in Col. 2

_ Please charge my Deposit Account No. 08-3038 in the amount of _____. A duplicate copy of this sheet is attached.

xx A check in the amount of $ 956.00 to cover the filing and assignment recordation fees is enclosed.

xx The U.S. Patent and Trademark Office is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 08-3038. A duplicate copy of this sheet is attached.

xx Any additional filing fees required under 37 CFR 1.16.
xx Any patent application processing fees under 37 CFR 1.17.

_ The U.S. Patent and Trademark Office is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 08-3038. A duplicate copy of this sheet is enclosed.

_ Any patent application processing fees under 37 CFR 1.17
_ The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).
_ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Date November 20, 1998

Joseph V. Colaianni, Jr. (Reg. No. 39,948)

WIRES FOR LIQUID CRYSTAL DISPLAYS, LIQUID CRYSTAL DISPLAYS HAVING THE SAME, AND MANUFACTURING METHODS THEREOF

BACKGROUND OF THE INVENTION

(1) Field of the invention

The present invention relates to wires for liquid crystal displays (LCDs), LCDs having the same and manufacturing methods thereof.

(2) Description of the Related Art

In general, an LCD has a gate wire on a substrate, and the gate wire includes gate lines, gate pads and gate electrodes which transmits scanning signals. The gate wire is covered with a gate insulating layer, and a semiconductor layer is formed on portions of the gate insulating layer opposite the gate electrodes. The LCD also has a data wire on the gate insulating layer, and the data wire includes data lines, data pads and source electrodes transmitting image signals and drain electrodes connected to the source electrodes through the semiconductor layer. A passivation layer having a contact hole exposing the drain electrode is formed on the data wire, and pixel electrodes which are formed of a transparent conductive material such as ITO (indium tin oxide) and connected to the drain electrodes through the contact hole are formed thereon.

To manufacture the liquid crystal display, deposition, photolithography and etch steps are required for the gate wire, the data wire, the gate insulating

layer, the passivation layer and the pixel electrodes.

There are two general methods for depositing a thin film, a chemical vapor deposition (CVD) and a physical deposition. The CVD forms the film by the reaction of vapor phase chemicals that contain the required constituents, while a sputtering which is a kind of physical deposition obtains the film by having energetic particles to strike target to be sputtered physically. The CVD is generally used to form the semiconductor layer and insulating layers such as the gate insulating layer and the passivation layer, and the sputtering is used to form metal layers for the gate wire and the data wire and an ITO layer for the pixel electrodes.

The etch method is divided into two types, wet etch using etchants and dry etch using etching gases.

In particular, when an ITO layer is etched by using an etchant, hydrochloric acid and nitric acid are used. However, it may happen that the etchant penetrates the passivation layer, contacts the data wire and the gate pad, and then erode the data wire and the gate pad. Accordingly, the data wire and the gate pad may be disconnected and/or eroded.

SUMMARY OF THE INVENTION

In view of the above, it is an object of the present invention to provide a data wire highly endurable against a chemical reactive etchant.

A wire according to the present invention is made of either molybdenum nitride layer or molybdenum alloy nitride layer.

The manufacturing method of the wires according to the present

invention uses a reactive sputtering method, and the target for the reactive sputtering may be made of a molybdenum alloy including one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %. The reactive gas mixture used for the reactive sputtering may include argon gas and nitrogen gas, and the inflow amount of the nitrogen gas is at least 50% of that of the argon gas.

Because the wires according to the present invention have low etch rate for the ITO etchant including strong acid, the disconnections of the wires are reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a layout view of a thin film transistor (TFT) array panel according to an embodiment of the present invention.

Figs. 2 and 3 show sectional views of the TFT array panel taken along the lines II-II' and III-III' in Fig. 1, respectively.

Figs. 4A-4F are sectional views of the intermediate structures of the TFT array panel shown in Fig. 1 to Fig. 3 manufactured by a manufacturing method according the embodiment of the present invention.

Fig. 5 is a graph illustrating etch rate of a molybdenum-tungsten alloy nitride layer as function of the volume of nitrogen gas as a reactive gas for aluminum and ITO etchants.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of

the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Fig. 1 shows a layout view of a TFT array panel according to an embodiment of the present invention, and Figs. 2 and 3 show sectional views taken along the lines II-II' and III-III' in Fig. 1, respectively.

The structure of the TFT array panel according to an embodiment of the present invention includes a supplementary wire highly endurable against a chemical reactive etchant to prevent disconnections of signal lines.

A gate wire made of either molybdenum or molybdenum alloy is formed on an insulating substrate 100, and the gate wire has a thickness of 1,000 - 4,000 Å and includes a transverse gate line 200, a gate electrode 210, which is a branch of the gate line 200, and a gate pad 230 which is connected to one end of the gate line 200. A supplementary gate wire 250 having a thickness of 300 - 1,000 Å is formed under the gate wire 200, 210 and 230 and made of

either molybdenum nitride (MoN_x) or molybdenum alloy nitride (Mo-alloy-N_x). The supplementary gate wire 250 may be located on the gate wire 200, 210 and 230. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium and nickel of the content of 0.1 to less than 20 atm %.

A gate insulating layer 300 covers the gate wire 200, 210 and 230, a hydrogenated amorphous silicon (a-si:H) layer 400 and a doped hydrogenated amorphous silicon layer 410 and 420 including N type impurity are sequentially formed on the gate insulating layer 300 opposite the gate electrode 210, and the portions 410 and 420 of the doped amorphous silicon layer are opposite each other with respect the gate electrode 220.

A data line 500 in the longitudinal direction is formed on the gate insulating layer 300, a source electrode 510 which is a branch of the data line 500 is formed on the one portion 410 of the doped amorphous silicon layer, and a drain electrode 520 opposite the source electrode 510 with respect to the gate electrode 210 is formed on the other portion 420 of the doped amorphous silicon layer. Here, the data wire including the data line 500, the source and drain electrodes 510 and 520 is made of either molybdenum or molybdenum alloy.

A supplementary data wire 550 made of either molybdenum nitride or molybdenum alloy nitride is formed under the data wire 500, 510 and 530. The molybdenum alloy used in this embodiment comprises one selected from tungsten, chromium, zirconium, and nickel of the content of 0.1 to less than 20

atm %. The supplementary data wire 550 may be located on the data line 500.

A passivation layer 700 is formed on the data wire 500, 510 and 520 and portions of the amorphous silicon layer 400 which is not covered by the data wire 500, 510 and 520. The passivation layer 700 has a contact hole C1 exposing the drain electrode 520, and another contact hole C2 exposing the gate pad 230 along with the gate insulating layer 300. Here, the description of a data pad connected to the data line 500 is omitted.

Finally, a pixel electrode 700 formed of ITO (indium tin oxide) and connected to the drain electrode 520 through a contact hole C1 is formed on the passivation layer 700. Furthermore, a gate ITO layer 710 connected to the gate pad 230 through the contact hole 720 and improving the contact characteristicis formed on the passivation layer 700.

A manufacturing method of the TFT array panel will now be described specifically with reference to Figs. 4A-4F.

Figs. 4A-4F show cross sectional views of the intermediate structures of the TFT array panel shown in Fig. 1 to Fig. 3 manufactured by a manufacturing method according the embodiment of the present invention.

As shown in Fig. 4A, a nitride layer 251 made of either molybdenum nitride or molybdenum alloy nitride is deposited on a transparent insulating substrate 100 by using reactive sputtering method. The target for the reactive sputtering is made of either molybdenum and molybdenum alloy having one selected from tungsten, chromium, zirconium, and nickel of the content ratio of 0.1 to less than 20 atm %. A reactive gas mixture includes argon gas (Ar) and

nitrogen gas (N_2), and the inflow amount of the nitrogen gas is equal to or more than 0.5 times that of argon gas. Thereafter, a metal layer 201 made of either molybdenum or molybdenum alloy is deposited by sputtering. The metal layer 201 may be deposited before the deposition of the nitride layer 251.

As shown in Fig. 4B, the metal layer 201 and the nitride layer 251 are sequentially patterned to form a gate wire including a gate line 200, a gate electrode 210 and a gate pad 230, and a supplementary gate wire 250 by performing a wet etch using an etchant such as aluminum etchant comprising nitric acid, acetic acid, phosphoric acid and dionized water.

As shown in Fig. 4C, a gate insulating layer 300 made from silicon nitride, a hydrogenated amorphous silicon layer and an extrinsic or doped hydrogenated amorphous silicon layer highly doped with N type impurity are sequentially deposited by plasma-enhanced chemical vapor deposition (PECVD hereafter). The amorphous silicon layer and the extrinsic amorphous silicon layer are patterned by photolithography to form an active pattern 401 and 411. A nitride layer 551 made of either molybdenum nitride or molybdenum alloy nitride with the thickness of 300~1,000 Å is deposited by using reactive sputtering method, and a metal layer 501 made of either molybdenum or molybdenum alloy with the thickness of 1,000 - 4,000 Å is deposited. The metal layer 501 may be deposited before the deposition of the nitride layer 551 When the thickness of the nitride layer 551 is less than 300 Å, it is difficult to obtain the uniform thickness, and the thickness of more than 1,000 Å is deteriorates the following etch step.

As shown in Fig. 4D, the metal layer 501 and the nitride layer 551 are sequentially patterned to form a data wire including a data line 500, a source electrode 510, a drain electrode 520 and a data pad (not shown), and a supplementary wire 550 by performing wet-etch using the above-described aluminum etchant. Because the etch rate for the upper metal layer 501 is larger than the etch rate for the low nitride layer 551, the metal layer 501 may be over-etched. Accordingly, it is desirable that the thickness of the nitride layer 551 is less than 1,000 Å to prevent the over-etch of the metal layer 501.

Thereafter, exposed portions of the extrinsic amorphous silicon layer 411 is removed such that the extrinsic amorphous silicon layer is then divided two portions 410 and 420, and the central portion of the amorphous silicon layer 400 is exposed.

As shown in Fig. 4E, a passivation layer 600 is deposited and patterned along with the gate insulating layer 300 to form contact holes C1 and C2 exposing the drain electrode 520 and the gate pad 230, respectively

Finally, an ITO layer is deposited and patterned to form a pixel electrode 700 connected to the drain electrode 520 through the contact hole C1 and a gate ITO layer 710 connected to the gate pad 230 through the contact hole 720 as shown in Fig. 4F. Here, the etchant for the ITO layer comprises hydrochloric acid and nitric acid, which may penetrate along the crack of the passivation layer 600 or along the edges of the ITO wire 700 and 710, and then may reach the data wire 500, 510 and 520, and the gate pad 230.

However, because the supplementary gate wire 250 and the

supplementary data wire 550 have a low chemical reactivation against the ITO etchant, the gate wire 200, 210 and 230, and the data wire 500, 510 and 520 through the supplementary gate wire 250 and the supplementary data wire 550 are not disconnected.

Next, the etch rate of a molybdenum-tungsten alloy nitride layer as function of volume of nitrogen gas as a reactive gas for aluminum and ITO etchants is described to confirm the low chemical reactivation of the supplementary gate and data wires 250 and 550 for aluminum and ITO etchants.

Fig. 5 is a graph illustrating etch rates of a molybdenum-tungsten alloy nitride layer as function of inflow amount of nitrogen gas as a reactive gas for aluminum and ITO etchants. The horizontal axis indicates the inflow amount of a nitrogen gas in sccm, and the vertical axis indicates etch rates of a molybdenum-tungsten alloy nitride layer in Å/sec for an aluminum etchant and an ITO etchants. In this experiment, the inflow amount 105 sccm of the Ar gas is fixed, and that of nitrogen gas varies from zero to 160 sccm during reactive sputtering. The etch rate of the molybdenum-tungsten alloy nitride layer for the aluminum etchant and the ITO etchant decreases as the inflow amount of nitrogen gas with respect to argon gas increases. Its etch rates for the aluminum etchant and the ITO etchant are respectively 95 Å/sec and 35 Å/sec when inflow amount of argon gas is 105 sccm and that of nitrogen gas is 50 sccm. The etch rate below 35 Å/sec implies that the etched thickness is negligible. In addition, because the mount of the ITO etchant penetrating

along the narrow crack having a width of less than 100 μm of the passivation layer is very small, the etched thickness of below 35 Å/sec is ignorable. In the meantime, the etch rate depends on the ratio of argon gas and nitrogen gas. For example, when the inflow amount of the nitrogen gas is at least 50 % of that of the argon gas, not only the supplementary gate and data wires 250 and 550 is simultaneously etched with the gate wire 200, 210 and 230, and the data wire 500, 510 and 520, but also the supplementary gate and data wires 250 and 550 is rarely etched for the ITO etchant.

In the drawings and specification, there have been disclosed typical preferred embodiments of the present invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

WHAT IS CLAIMED IS:

1. A manufacturing method of a molybdenum-metal alloy nitride layer by a reactive sputtering using argon gas and nitrogen gas as a reactive gas mixture:

wherein a target for the reactive sputtering is made of molybdenum alloy comprising a metal of 0.1 to less than 20 atm %, and inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

2. The method of the claim 1, wherein the metal is one selected from the group consisting of tungsten, chromium, zirconium and nickel.

3. A molybdenum-metal alloy nitride layer manufactured by the method of claim 2.

4. A wire for a display liquid display comprising:

a main layer made of either molybdenum or molybdenum alloy;

a supplementary layer which is located either on or under the main layer and made of either molybdenum nitride or molybdenum alloy nitride.

5. The wire of claim 4, wherein the supplementary layer comprises one selected from the group consisting of tungsten, chromium, zirconium and nickel.

6. A manufacturing method of a wire for a liquid crystal display comprising the steps of:

depositing a first layer made of either molybdenum or molybdenum alloy on a substrate;

depositing a second layer made of either molybdenum nitride or molybdenum alloy nitride by using reactive sputtering, and

patterning simultaneously the second and the first layers.

7. The manufacturing method of claim 6, wherein a target for the reactive sputtering is made of either molybdenum or molybdenum alloy, and

the molybdenum alloy comprises one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %

8. The manufacturing method of claim 7, wherein a reactive gas mixture for the reactive sputtering includes argon gas and nitrogen gas, and the nitrogen gas inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

9. The manufacturing method of claim 8, wherein the thickness of the second layer is 300 to 1,000 Å.

10. A manufacturing method of a wire for a liquid crystal display comprising the steps of:

depositing a first layer made of either molybdenum nitride or molybdenum alloy nitride by using reactive sputtering;

depositing a first layer made of either molybdenum or molybdenum alloy on a substrate; and patterning simultaneously the second and the first layers.

11. The manufacturing method of claim 10, wherein a target for the reactive sputtering is made of either molybdenum or molybdenum alloy, and

the molybdenum alloy comprises one selected from tungsten, chromium, zirconium and nickel of 0.1 to less than 20 atm %.

12. The manufacturing method of claim 11, wherein a reactive gas mixture for the reactive sputtering includes argon gas and nitrogen gas, and the nitrogen gas inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

13. The manufacturing method of claim 12, wherein the thickness of the first layer is 300 to 1,000 Å.

14. A display liquid display comprising:

an insulating substrate;

a gate wire formed on the substrate;

a gate insulating layer covering the gate wire;

a data wire which is made of one of either molybdenum or molybdenum alloy and formed on the gate insulating layer;

a supplementary data wire which is located either on or under the data wire and made of either molybdenum nitride or molybdenum alloy nitride;

a passivation layer formed on the data wire or the supplementary data wire; and

an ITO pixel electrode formed on the passivation layer and connected to the data wire through contact formed in the passivation layer.

15. The liquid crystal display of claim 14, wherein the supplementary data wire comprises one selected from the group consisting of tungsten, chromium, zirconium and nickel

16. The liquid crystal display of 17, further comprising:

a supplementary gate wire which is located either on or under the gate wire and made of either molybdenum nitride or molybdenum alloy nitride.

17. The liquid crystal display of claim 18, wherein the supplementary gate wire comprises one selected from the group consisting of tungsten, chromium, zirconium and nickel.

18. A manufacturing method of a liquid crystal display comprising the steps of:

forming a gate wire on a substrate;

forming a gate insulating layer on the gate wire;

forming a semiconductor layer on the gate insulating layer;

depositing a first layer made of either molybdenum or molybdenum alloy;

depositing a second layer made of either molybdenum nitride or molybdenum alloy nitride by using reactive sputtering method;

patterning simultaneously the second and the first layer to form a data wire and a supplementary data wire;

forming a passivation layer on the data wire or the supplementary data wire; and

forming a pixel electrode made of ITO.

19. The manufacturing method of claim 18, wherein a target for the reactive sputtering is made of either molybdenum or molybdenum alloy, and

the molybdenum alloy comprises one selected from tungsten,

chromium, zirconium and nickel of 0.1 to less than 20 atm %.

20. The manufacturing method of claim 21, wherein a reactive gas mixture for the reactive sputtering includes argon gas and nitrogen gas, and the nitrogen gas inflow amount of the nitrogen gas is at least 50% of the inflow amount of the argon gas.

ABSTRACT OF THE DISCLOSURE

A wire for a liquid crystal display has a dual-layered structure comprising a first layer made of molybdenum or molybdenum alloy, and a second layer made of molybdenum nitride or molybdenum alloy nitride. To manufacture the wire, a layer made of either a molybdenum or a molybdenum alloy, and another layer one of either a molybdenum nitride or molybdenum alloy nitride by using reactive sputtering method are deposited in sequence, and then patterned simultaneously. The target for reactive sputtering is made of either molybdenum or molybdenum alloy, and the molybdenum alloy comprises one selected from the group consisting of tungsten, chromium, zirconium, and nickel of the content ratio of 0.1 to less than 20 atm % of. The reactive gas mixture for reactive sputtering includes an argon gas and inflow amount of the nitrogen gas is at least 50% of argon gas, to minimize the etch rate of the molybdenum nitride layer or the molybdenum alloy nitride layer for ITO etchant.

Fig. 1

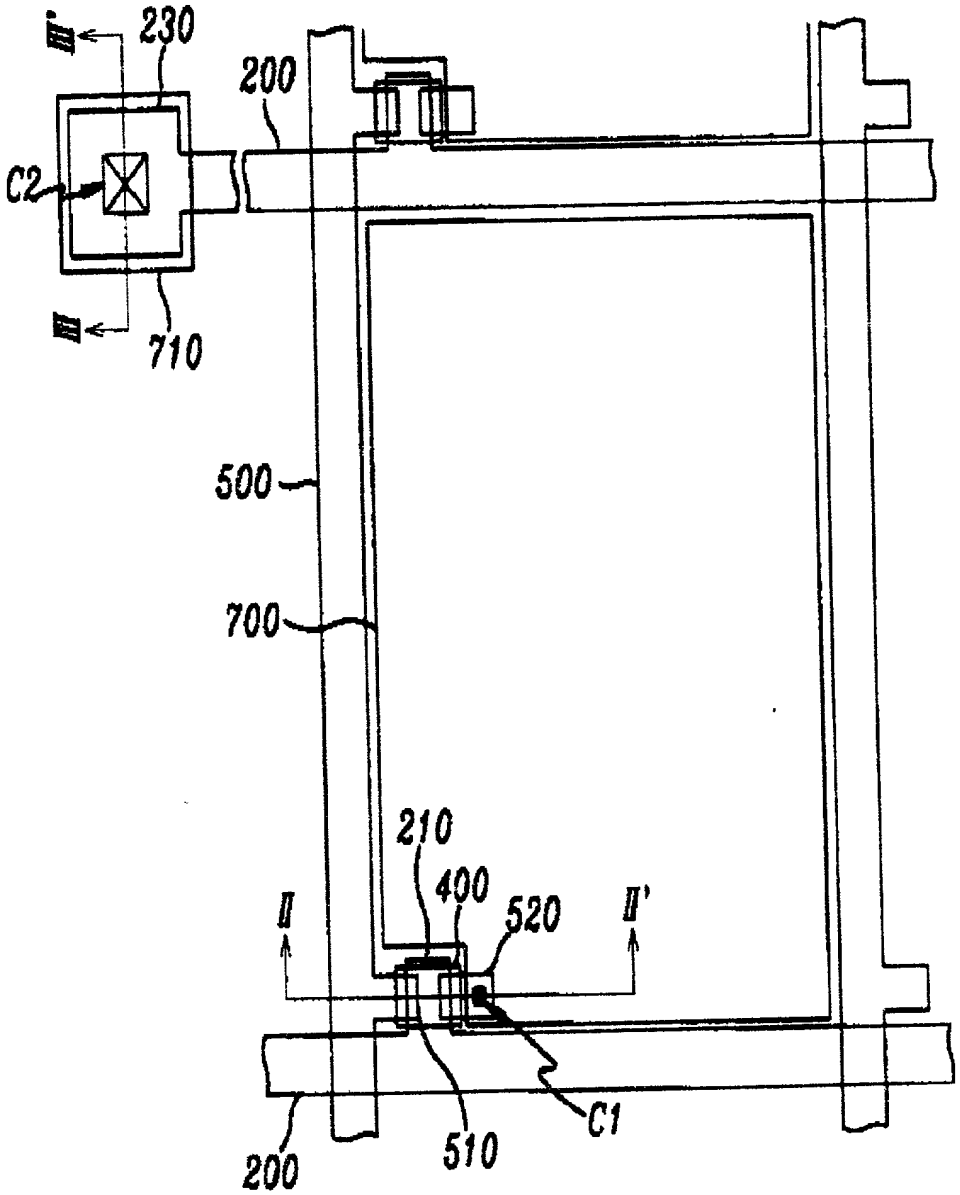

Fig. 2

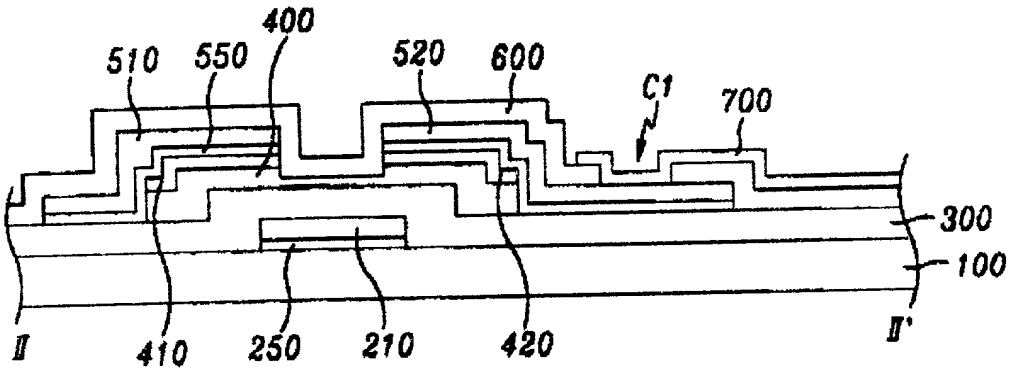
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Fig. 3

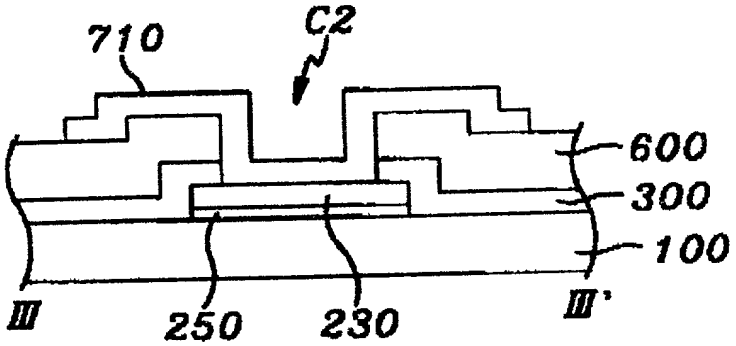

710
C2
600
300
100
III
250
230
III'

Fig. 4A

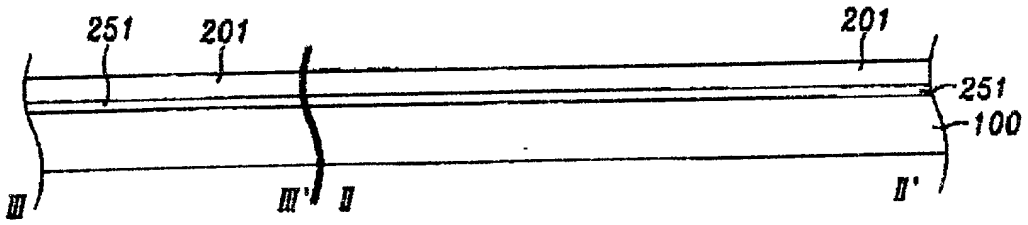

251
201
201
251
100
III
III'
II
II'

Fig. 4B

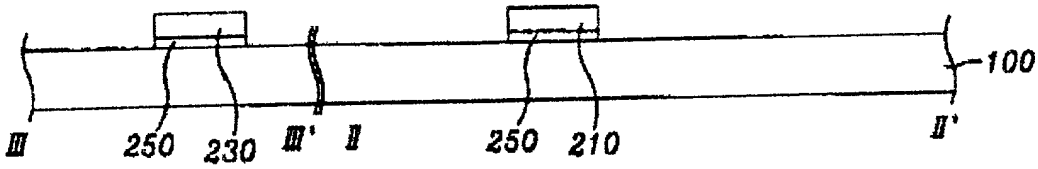

100
III
250
230
III'
II
250
210
II'

Fig. 4C

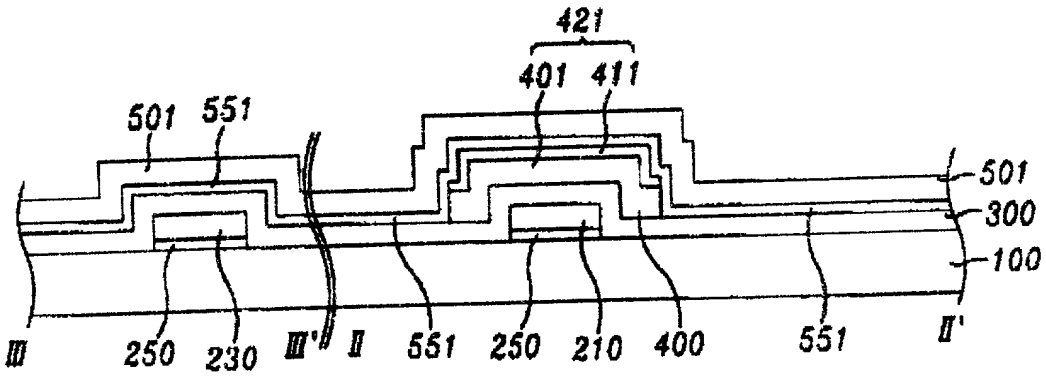

421
401
411
501
551
501
300
100
III
250
230
III'
II
551
250
210
400
551
II'

Fig. 4D

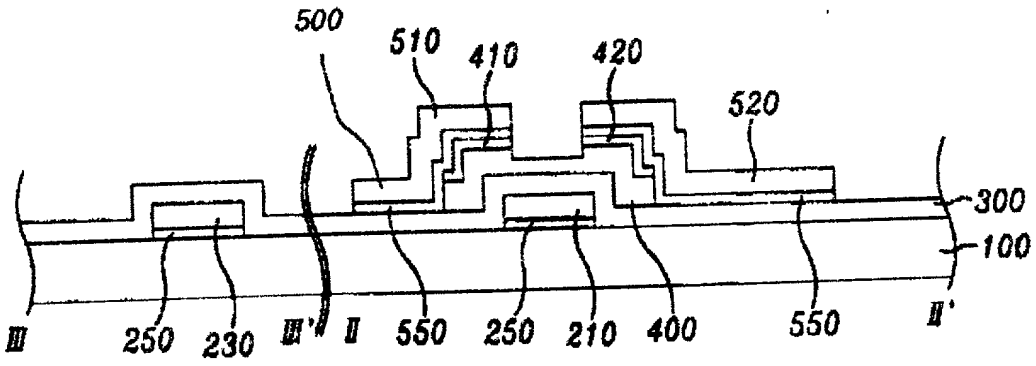

500
510
410
420
520
300
100
III
250
230
III'
II
550
250
210
400
550
II'

Fig. 4E

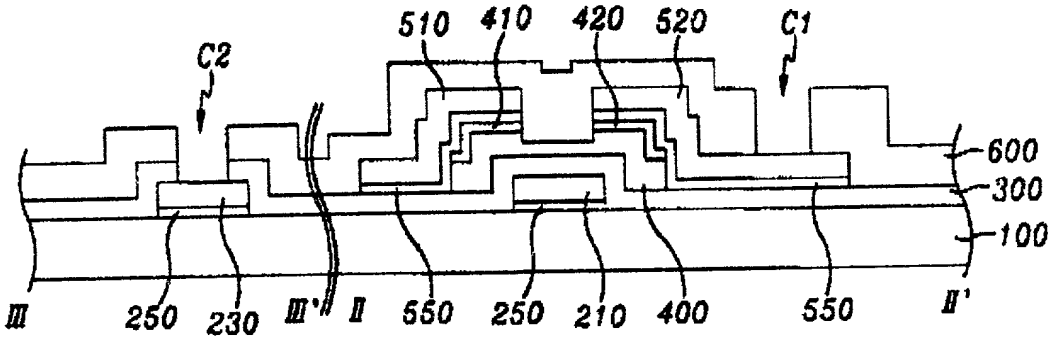

510
410
420
520
C1
C2
600
300
100
III
250
230
III'
II
550
250
210
400
550
II'

Fig. 4F

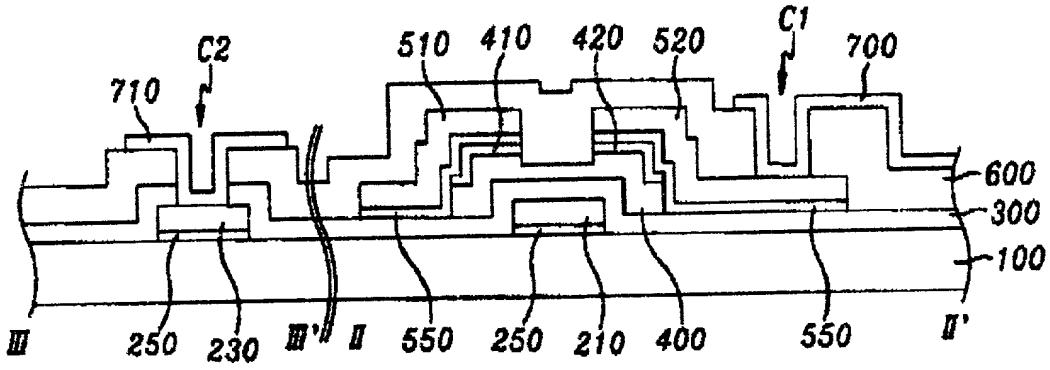
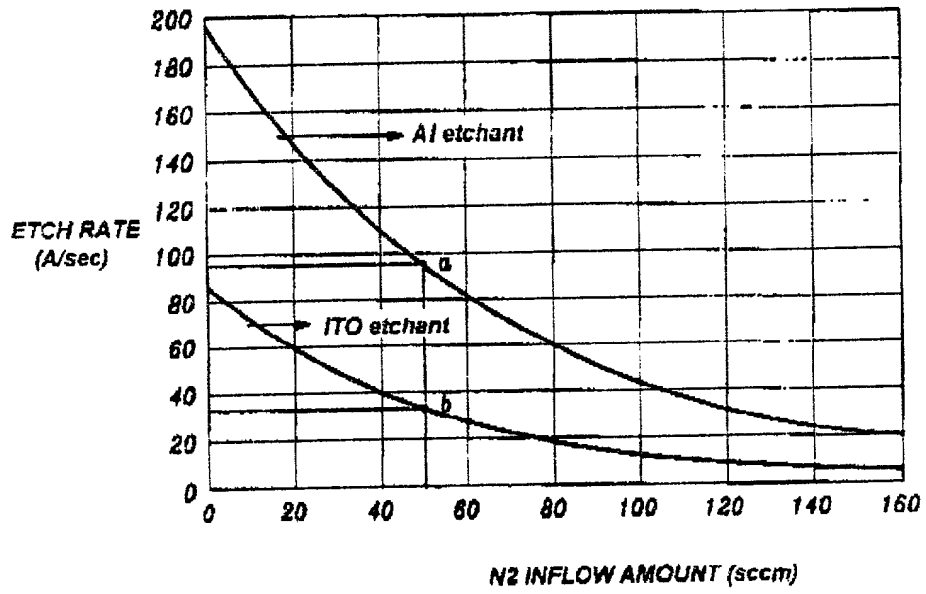

C1
700
510
410
420
520
C2
710
600
300
100
III
250
230
III'
II
550
250
210
400
550
II'

Fig. 5


ETCH RATE
(A/sec)
200
180
160
140
120
100
80
60
40
20
0
Al etchant
ITO etchant
a
b
0
20
40
60
80
100
120
140
160
N2 INFLOW AMOUNT (sccm)

Combined Declaration and Power of Attorney for Patent Application

Docket Number.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled **WIRES FOR LIQUID CRYSTAL DISPLAYS, LIQUID CRYSTAL DISPLAYS HAVING THE SAME, AND MANUFACTURING METHODS THEREOF**, the specification of which is attached hereto unless the following box is checked:

☐ was filed on ___/___/___
as United States Application Number or PCT International Application Number ___ ; and
was amended on ___/___/___ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
			☒ Yes ☐ No
97-61315 (Application No.)	KOREA (Country)	20/11/1997 (Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application No.) (Filing Date)

(Application No.) (Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application No.) (Filing Date) (Status - patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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